



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:

Wilbur Catabay
Richard Schinella
Zihai Wang
Wei-Jen Hsia

Serial No.: 10/614,776

Filed: July 07, 2003

For: Process for Planarizing Upper
Surface of Damascene Wiring
Structure For Integrated Circuit
Structures

Group Art Unit: 2813

Examiner: Blum, David

Atty Docket: / 01-212/1P

I hereby certify that this correspondence is being deposited with the U.S.
Postal Service as First Class Mail in an envelope addressed to: Commissioner
for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Connie Del Castillo

01/26/05 ConnieDelCastillo

Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 24 Jan 05

Respectfully submitted,

Timothy Croll

Reg. No. 36,771